IN THE SPECIFICATION

Please replace the paragraph 19 on page 7 with the following amended paragraph.

The operation of the SLOS circuit will be described hereinafter in connection with the timing diagram shown in FIG. 2 and the exemplary SLOS circuit shown in FIG. 3. For illustrative purposes, an exemplary SONET OC-192 application will be assumed wherein the SLOS circuitry receives a 10 Gb/s incoming data and a 10 GHz extracted clock signal. It is to be understood, however, that the invention is not limited to any specific telecommunication standard. Referring to FIG. 2, the top two waveforms show DataIn and CLK signals. As noted therein, at 10 GHz, the clock period T equals 100 ps. Thus, in the exemplary embodiment where buffer 110 delays DataIn by T/4, the delay would be 25 ps. Referring to FIG. 3, f/f 108 latches the 10 GHz extracted clock signal CLK using the delayed data (signal DataIn_Delayed in FIG. 2). An error count occurs when an edge of the incoming data drifts past the allowed window ΔT on either ~~sides~~ side of the falling edge of CLK (when CLK falling edge is used to sample the data eye). That is, the SLOS circuitry needs to detect for both conditions $(T/2)\pm\Delta T$. Denoting the phase relationship between CLK and DataIn by τ_{D2C}, the output of f/f 108, Qb, would depend on τ_{D2C}. If τ_{D2C} is less than T/4 or larger than 3T/4, then Qb would be, e.g., high, otherwise it would be low as shown in FIG. 2. FIG. 2 illustrates all three cases; when τ_{D2C} is greater than T/4 ($\tau_{D2C} > T/4$; no error detected), when τ_{D2C} is larger than 3T/4 ($\tau_{D2C} > 3T/4$; error detected), and when τ_{D2C} is smaller than T/4 ($\tau_{D2C} < T/4$; error detected).

Please replace paragraph 20 on page 8 with the following amended paragraph.

Referring to the example shown in FIG. 2, τ_{D2C} is defined by the time duration between a transition in DataIn and the next falling edge of CLK. The first transition on DataIn_Delayed at time t1 that clocks f/f 108 occurs at about the middle of the positive half-cycle of CLK. In this instance, the relationship $\tau_{D2C} > T/4$ clearly holds resulting in Qb being low (Qb is the complementary output of f/f 108). The same is true for the next transition of DataIn_Delayed at time t2 when f/f 108 latches a high value presented by CLK, resulting in Qb being low. Referring now to FIG. 3, there is shown an exemplary implementation for integrator 112 in greater detail. Integrator 112 includes a switch S1 that when closed connects a current source I_0 to a capacitor C. The top plate of capacitor C provides the signal V_{BER} and connects to one input of comparator

114. Accordingly, as long as Qb remains low, switch S1 ~~is~~ remains open and capacitor C remains discharged, maintaining a low state for V_{BER}.